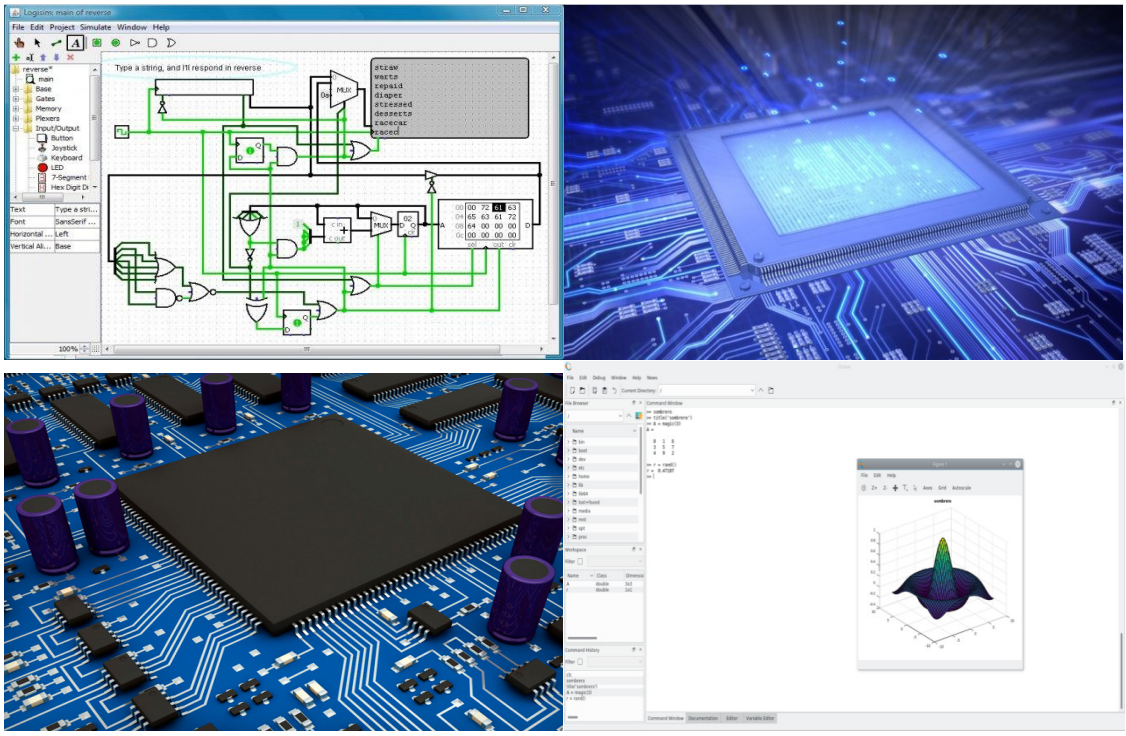
Curriculum & Contents

# M. Tech.
# (IC Design and Technology)



विश्वजीवनामृतं ज्ञानम्

ABV-Indian Institute of Information Technology & Management, Gwalior

# M. Tech. (IC Design and Technology)
# Department of Electrical and Electronics Engineering

**Total credits – 21+21+18+18 = 78**

**Exit After First Year: PG Diploma in IC Design and Technology**

## Semester-wise Subject Allocation:

| Semester I | | | | |
|---|---|---|---|---|
| **S. No.** | **Subject Code** | **Title of the course** | **L-T-P** | **Credits** |
| 1 | EE-601 | Digital IC Design | 3-0-0 | 3 |
| 2 | EE-602 | System Design using HDL | 3-0-0 | 3 |
| 3 | EE-603 | CAD for VLSI | 3-0-0 | 3 |
| 4 | EE-604 | IC Technology | 3-0-0 | 3 |
| 5 | EE-605 | Device Modelling and Simulation | 3-0-0 | 3 |
| 6 | EE-606 | Advanced IC Design and Technology Lab-1 | 0-1-4 | 3 |
| 7 | EE-XXX | Elective 1 | 3-0-0 | 3 |
| | | | Total credits | 21 |
| Semester II | | | | |
| 1 | EE-607 | Analog IC Design | 3-0-0 | 3 |
| 2 | EE-608 | Design Verification and Testing | 3-0-0 | 3 |
| 3 | EE-609 | Engineering Research Methodology | 2-0-0 | 2 |
| 4 | EE-610 | Machine Learning | 3-0-2 | 4 |
| 5 | EE-611 | Advanced IC Design and Technology Lab-II | 0-1-4 | 3 |
| 6 | EE-XXX | Elective- II | 3-0-0 | 3 |
| 7 | EE-XXX | Elective-III | 3-0-0 | 3 |
| | | | Total credits | 21 |

| Semester III | | | | |
|---|---|---|---|---|
| **S. No.** | **Subject Code** | **Title of the course** | **L-T-P** | **Credits** |
| **1** | **XXX** | **Elective-IV/MOOC course** | **3-0-0** | **3** |
| **2** | **XXX** | **Elective-V/MOOC course** | **3-0-0** | **3** |
| **3** | **EE-698** | **Major Project part I/Internship** | **-** | **12** |
| | | | **Total credits** | **18** |

| Semester IV | | | | |
|---|---|---|---|---|
| **S. No.** | **Subject Code** | **Title of the course** | **L-T-P** | **Credits** |
| **1** | **XXX** | **Elective-VI/MOOC course** | **3-0-0** | **3** |
| **2** | **EE-699** | **Major Project part II/Internship** | **-** | **15** |
| | | | **Total credits** | **18** |

## List of Electives for IC Design and Technology

| S. No. | Subject Code | Course | L-T-P | Credits |
|---|---|---|---|---|
| 1. | EE-051 | Device and interconnect modelling | 3-0-0 | 3 |
| 2. | EE-052 | VLSI Signal Processing | 3-0-0 | 3 |
| 3. | EE-053 | Low Power VLSI | 3-0-0 | 3 |
| 4. | EE-054 | Microcontroller and Embedded Systems | 3-0-0 | 3 |
| 5. | EE-055 | Memory Devices and Circuits | 3-0-0 | 3 |
| 6. | EE-056 | VLSI Architecture | 3-0-0 | 3 |
| 7. | EE-057 | Hardware Security | 3-0-0 | 3 |
| 8. | EE-058 | FPGA Based System Design | 3-0-0 | 3 |
| 9 | EE-059 | Quantum Electronics | 3-0-0 | 3 |
| 10 | EE-060 | RF Circuit Design | 3-0-0 | 3 |
| 11 | EE-061 | Mixed Signal SoC Design | 3-0-0 | 3 |
| 12 | EE-062 | AI-Accelerator Design | 3-0-0 | 3 |
| 13 | EE-063 | System-on-Performance Chip Design | 3-0-0 | 3 |
| 14 | EE-064 | Embedded Software | 3-0-0 | 3 |
| 15 | EE-065 | High Performance Computing Systems | 3-0-0 | 3 |
| 16 | EE-066 | Special Topics in IC Design and Technology | 3-0-0 | 3 |
| 17 | EE-067 | Sensors for autonomous system | 3-0-0 | 3 |
| 18 | EE-068 | Network on Chip | 3-0-0 | 3 |

# Course Contents

| | | |
|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |
| 3 | **Codeofthesubject** | EE-601 |
| 4 | **Titleofthesubject** | Digital IC Design |
| 5 | **Anyprerequisite** | NIL |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectivesof the subject** | This course aims to convey knowledge of basic concepts of digital VLSI circuit design using CMOS and state-of-the-art device technologies with an emphasis on "hands-on" IC design using ECAD/CAD tools. Emphasisisonthecircuitdesign, optimization, and layout of very high speed, high density or low power circuitsfor use in applications such as processors, signal and memory and periphery. Specialattention will be devoted to the most important challenges facing digital circuit designerstoday and in the coming decade, being the impact of scaling, deep submicron effects,interconnect,signalintegrity,power distributionandconsumption for energy efficient and PVT aware real-time applications.<br>Students should be able to apply their knowledge of electronics and engineering in thedesignofCMOSintegrated circuitsand digitalVLSI design as per the need of current academia and VLSI industry. |
| 8 | **Brief Contents** | Introductionandfutureprospects, Evolutionof CMOS transistorstructure, Modelingof transistor using SPICE, Inverters static characteristics, Inverterssswitchingcharacteristicsandinterconnecteffects;<br>Combinationallogiccircuits, Sequentiallogiccircuits, Dynamiclogic circuits, Semiconductormemories, Low powerlogiccircuits, High-speed circuits |

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|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |
| 3 | **Code of the subject** | EE-602 |
| 4 | **Title of the subject** | System Design using HDL |
| 5 | **Any prerequisite** | Digital Electronics in UG |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectives of the subject** | Correctly describe the detailed behaviour of given standard and few special application based digital logic circuits as defined by Verilog HDL, state diagrams, or other means, including those circuits related to modern computer architecture.<br>Translate system requirements into a practical digital design using Verilog HDL, Xilinx Vivado, and FPGA prototyping boards.<br>Model the digital designs including FSMs to Processor architectures using the knowledge of HDL Language.<br>Apply the knowledge of Reconfigurable architectures like FPGAs in designing and implementing digital ICs. |
| 8 | **Brief Contents** | Basic concepts of hardware description languages (VHDL, Verilog HDL), Logic and delay modeling, Structural, Data-flow and Behavioral styles of hardware description, Architecture of event driven simulators, Operators, Operands, Operator types, Blocking and non-blocking statements, Delay control, Generate statement, Event control, Sequential Logic Design, FSM, Configuration Specifications, Sub-Programs, Test Benches.<br>Types of Reconfiguration, Details study of FPGA, Design tradeoffs, Bidirectional wires and switches, FPGA Placement: Placement Algorithms, FPGA Routing, Timing Analysis, Network Virtualization with FPGAs, On-chip Monitoring Infrastructures, Multi-FPGA System Software, Logic Emulation, Applications, High Level Compilation |

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|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |
| 3 | **Codeofthesubject** | EE-603 |
| 4 | **Titleofthesubject** | CADfor VLSI |
| 5 | **Anyprerequisite** | DigitalDesign |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectives of the subject** | The main objective of this course is to provide in-depth understanding of thetheoreticalaswellaspracticalconceptsofthedesigningalgorithmsfor CADtoolsfor VLSI design. The students will be able to identify and develop new algorithmsand CAD tools for VLSI design. The scope of this course is also to visualize newDesign Automation (DA) research problems in view of the challenges ofdesigning multi-core and/or many-core system-on-chip in the nanometer regime.Another objective of this course is to give the exposure to machine learning anddeep learningalgorithmsfordesigningefficienthardwarein IOTera. |
| 8 | **BriefContents** | Introduction to VLSI-CAD, modulegeneration,PLAsandFPGAs, Digitalhardware modeling, benchmarkcircuits(ISCAS'85, ISCAS'89…), Simulation algorithms design verification, graphdatastructureandalgorithmsfor VLSI-CAD, High-level synthesis, Algorithms for physical design automation, slicingand non-slicing floorplans, polar graphs and adjacency graphs for floorplans, IntroducingNOCasafutureSOCparadigm, Timing analysis, SDC, set-up & hold time concept, timing exceptions, set-up & hold calculations, noise analysis. |

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|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |
| 3 | **Code of the subject** | EE-604 |
| 4 | **Title of the subject** | IC Technology |
| 5 | **Any prerequisite** | Nil |
| 6 | **L.T.P.** | 3-0-0 |
| 7 | **Learning Objectives of the subject** | Students will be able to learn the flow of IC Design which includes fundamental of fabrication of chip, input output packaging, interconnection network.<br>To demonstrate a clear understanding of CMOS fabrication flow, input/output circuits, chip packaging.<br>Get the idea of data flow in interconnection network, routing and topology basics. |
| 8 | **Brief Contents** | Chip Design flow using Full custom, Semicustom approach<br>CMOS Technology, GaAs Technology, Bipolar-CMOS-DMOS (BCD) Technology, Advanced Process Technology<br>CMOS Process flow, IC Manufacturing, Input Output Interfacing, Input Circuits, Output circuits, ESD, Packaging, Signal Integrity.<br>Electrical Testing, Yield, Future trends, and Challenges: Challenges for integration, system on chip, Novel Devices.<br>Chip packaging |

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|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |
| 3 | **Codeofthesubject** | EE-605 |
| 4 | **Titleofthesubject** | Device ModellingandSimulation |
| 5 | **Anyprerequisite** | ElectronicsDevicesandCircuits |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectivesof the subject** | Theobjectiveofthecourseistoprovidethefundamentalknowledgeforunderstanding the basic conceptsofsemiconductordevices.<br>Uponsuccessfulcompletionofthecourse,studentswillbeabletograspfundamentalknowledgeofsemiconductordevicesforIntegratedCircuitdesign.<br>Beabletomodelthedevices and circuits usingSPICE. |
| 8 | **BriefContents** | Device Level Modeling: PN Junction, MOSFET, Limitationoflongchannelanalysis,Short-channeleffects, Technology nodes and ITRS, Physical& technological challenges to scaling, nonconventional MOSFET (FDSOI, SOI,Multi-gateMOSFETs), Compact modelling, Verilog-A model<br>Interconnect Modelling: Introduction to VLSI Interconnects. Distributed RC interconnect model, Elmore delay, Equivalent Elmore model for RLC interconnects (Distributed model), Two-pole model of RLC interconnects from ABCD parametersCircuit Modelling: Circuit simulation using available device model, Netlist, System Modelling: |

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|---|---|---|
| 1 | **Semester** | I |
| 2 | **Type of course** | Core |

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|---|---|---|
| 3 | **Codeofthesubject** | EE-606 |
| 4 | **Titleofthesubject** | Advanced IC Design and TechnologyLab-I |
| 5 | **Anyprerequisite** | NIL |
| 6 | **L-T-P** | 0-1-4 |
| 7 | **Learning Objectivesof the subject** | The lab experiments of this course will provide an exposure how the fundamental and advanced theory, design concepts, principles of the core courses studied in 1st semester can be applied in practice. Theobjectiveofthecourseistoprovidethefundamentalknowledgefor understanding the flow of IC Design using EDA tool and further better approaches/solutions for more effective design.<br>The fundamentals of HDL language, concept to design the system using the HDL Language and implementation of the design on FPGA Boards. RTL to GDS flow which will cover the basic concepts of physical design.<br>Uponsuccessfulcompletionofthecourse,studentswillbeabletograspfundamentalsteps and flow of IC Design using EDA tools. |
| 8 | **BriefContents** | The complete IC layout design and its implementation using EDA tool. Provide the in-depth concept and flow for implementation of IC Design, CMOS logic, Circuit analysis with change in the device parameters, Impact of parasitics on circuit performance.<br><br>Fundamentals of Verilog HDL, different levels of abstraction, tasks and directives, Concept to design the FSM and microarchitecture, Timing and delay simulations,Fundamentals of Physical Design during RTL to GDS flow, Physical Synthesis. |
| 9 | **Contents for lab** | Schematic and Layout analysis of inverter, AND gate, OR gate, NAND gate, NOR gate, XOR gate and XNOR gate (pre layout simulation and post layout simulation), IC fabrication process.<br><br>Implementation of all the basic and universal gates using HDL, combinational circuits, sequential circuits, FSM implementation, memory design, Micro-architecture implementation.Automation of FPGAs.Physical Design, Partitioning, Floor plan, Placement and Routing, Timing analysis |

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| 1 | **Semester** | II |
| 2 | **Type of course** | Core |

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|---|---|---|
| 3 | **Code of the subject** | EE-607 |
| 4 | **Title of the subject** | Analog IC Design |
| 5 | **Any prerequisite** | Digital IC Design |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectives of the subject** | On completion of this course, the students will be able to:<br>Acquire a basic knowledge of analog IC design including small signal models, and analog MOS processes.<br>Design of single stage and differential stage amplifiers with and without current mirror circuits, respectively.<br>Analyze the frequency responses of single-stage amplifiers.<br>Analyze and design two-stage operational amplifier.<br>Identify the different types of noises in analog integrated circuits. |
| 8 | **Brief Contents** | Small signal Models, Amplifiers and Current sources: Large Signal and Small-Signal analysis of common source stage, Source Follower, Common Gate Stage, Cascode, Folded Cascode, Differential amplifier, current Sources, Basic Current Mirrors, Cascode Current Mirrors and current mirror based differential amplifier, Frequency Response of Amplifiers, Feedback, Operational Amplifier, Noise, Determination of dominants poles; Compensation and relocation of poles and zeros,<br>Basic concepts to design PLL and ADC |

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| 1 | **Semester** | II |
| 2 | **Type of course** | Core |

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|---|---|---|
| 3 | **Code of the subject** | EE-608 |
| 4 | **Title of the subject** | Design Verification and Testing |
| 5 | **Any prerequisite** | CAD for VLSI |
| 6 | **L-T-P** | 3-0-0 |
| 7 | **Learning Objectives of the subject** | The main objective of this course is to provide in-depth understanding of the problems encountered in testing large circuits, approaches to detect and diagnose the faults and methods to improve the design to make it testable. The students will be able to develop algorithms and tools for VLSI testing, designing of testable and trustworthy circuits. The scope of this course is to particularly address the challenges in the VLSI testing domain and get motivated towards research in this field. |
| 8 | **Brief Contents** | Introduction and Fault Modeling, Testing Techniques, Time frame expansion methods, Boolean Satisfiability, Transitive-closure based and Neural Network based approaches, Fault Simulation, Design for Testability and Built-in-self-test, Controllability and observability measures, TEMEAS, SCOAP, Ad-hoc design built-in-logic-block-observer (BILBO), Linear feedback shift register (LFSR), Theory of LFSRs, Design for Trust Techniques: Different Types of Attacks, Counter Measures for different types of attacks, Prevention based Approaches, Importance of verification, Verification plan, Verification flow, Levels of verification, Verification methods and languages, Introduction to Hardware Verification methodologies, Verifications based on simulation, Analytical and formal approaches. Functional verification, Timing verification, Formal verification. Basics of equivalence checking and model checking |

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| 1 | **Semester** | II |

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|---|---|---|
| 2 | **Type of course** | Core |
| 3 | **Code of the subject** | EE-609 |
| 4 | **Title of the subject** | Engineering Research Methodology |
| 5 | **Any prerequisite** | NIL |
| 6 | **L-T-P** | 2-0-0 |
| 7 | **Learning Objectives of the subject** | Demonstrate the ability to choose appropriate methods for research aims and objectives. Understand the limitations of particular research methods. Develop skills in qualitative and quantitative data analysis and presentation. Develop advanced critical thinking skills.<br><br>The main objective of this course is to introduce the basic concepts in research methodology in Science, Engineering and Technology. This course addresses the issues inherent in selecting a research problem and discuss the techniques and tools to be employed in completing a research project. This will also enable the students to prepare report writing and framing Research proposals for their course projects, internship projects and dissertations. |
| 8 | **Brief Contents** | Introduction to research - Research Methods in Engineering, Research paper analysis, Data analysis of reported data, Advance trends in electrical and electronics engineering, Review Process, Review guidelines, Qualitative Methods, Study Designs, The nature and types of qualitative research, Survey Study Designs, Case Studies. Introduction to Mixed Methods Research, Study Designs and Method. Cutting edge challenges and their solution. Writing research papers, purpose, nature and evaluation, content and format, Research Presentations, The Art of Scientific and Technical Writing. |

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| 1 | **Semester** | II |

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| 2 | **Type of course** | Core |
| 3 | **Code of the subject** | EE-610 |
| 4 | **Title of the subject** | Machine Learning |
| 5 | **Any prerequisite** | NIL |
| 6 | **L-T-P** | 3-0-2 |
| 7 | **Learning Objectives of the subject** | To understand popular ML algorithms with their associated mathematical foundations for appreciating these algorithms, To help connect real-world problems to appropriate ML algorithm(s) for solving them and to enable formulating real world problems as machine learning tasks |
| 8 | **Brief Contents** | Introduction to ML, Fundamentals of ML - PCA and Dimensionality Reduction,Nearest Neighbours and KNN, Linear Regression, Decision Tree Classifiers. Notion of Generalization and concern of Overfitting, Notion of Training, Validation and Testing; Connect to generalisation and overfitting. Selected Algorithms - Ensembling and RF, Linear SVM, K Means,Logistic Regression, Naive Bayes,Neural Network Learning - Role of Loss Functions and Optimization, Gradient Descent and Perceptron/Delta Learning, MLP, Backpropagation, MLP for Classification and Regression, Regularisation, Early Stopping,Kernels (with SVM), Bayesian Methods, Generative Methods, HMM, EM, PAC learning,Introduction to Deep Learning, CNNs, Popular CNN Architectures, RNNs, Advances in Backpropagation and Optimization for Neural Networks Adversarial Learning. |
| 9 | **Contents for lab** | To implement basic algorithms using standard machine learning libraries. Gainhands-on experience in applying ML to problems encountered in various domains. In addition, obtain exposure to provide solutions for complex and special application based problems using high-level ML libraries or frameworks such as TensorFlow, PyTorch. |

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| 1 | **Semester** | II |

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|---|---|---|
| 2 | **Type of course** | Core |
| 3 | **Codeofthesubject** | EE-611 |
| 4 | **Titleofthesubject** | Advanced IC Design and TechnologyLab-II |
| 5 | **Anyprerequisite** | NILL |
| 6 | **L-T-P** | 0-1-4 |
| 7 | **Learning Objectivesof the subject** | The lab experiments of this course will provide an exposure how the fundamental and advanced theory, design concepts, principles of the core/elective courses studied in 2nd semester can be applied in practice.<br><br>Theobjectiveofthecourseistoprovidethefundamentalknowledgefor understanding the flow of IC Design using EDA tool and further better approaches/solutions for more effective design.<br><br>Theobjectiveofthecourseistoprovidethefundamentalknowledge of Analog IC Design using Cadence EDA tool.<br>In-depth introduction to the SystemVerilog,efficient verification using SystemVerilog. |
| 8 | **BriefContents** | Design steps to implement the Analog circuits using EDA tools, Provide the in-depth concept and flow for implementation of IC Design, Circuit analysis with change in the device parameters, Impact of parasitics on circuit performance.<br><br>Improvements for RTL design and synthesis;<br>Verification enhancements such as object-oriented design;<br>Assertions and randomization. |
| 9 | **Contents for lab** | SystemVerilog RTL design and synthesis including different data types, literals, procedural blocks, statements, and operators. Tasks and functions, hierarchy and connectivity features, and interfaces. Classes, constrained random stimulus, coverage, strings, queues and dynamic To draw the schematic, perform simulation and find the gain for common source, common drain and common gate amplifier. The layout of the same, simulate the layout for ac analysis and comment on the results.Design a current mirror circuit and verify its operation.<br>Design an active load single-stage amplifier.Design a differential amplifier and find out the gain. Op-amp design and analysis. Design of PLL and ADC for mixed signal SoC applications |
| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-051 |

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|---|---|---|
| 3 | **Titleofthesubject** | Device and Interconnect Modelling |
| 4 | **Anyprerequisite** | NIL |
| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectivesof the subject** | Upon the completion of this course, the students willbe able to:<br>Apply the concept of MOS modelling in IC design<br>Understand the advanced interconnect materials.<br>Acquire knowledge about Technology trends, Device and interconnect.<br>scaling.<br>Identify basic device and Interconnect Models.<br>Perform RLC based Interconnect analysis.<br>Analyse the problem with existing material in deep submicron. |
| 7 | **BriefContents** | Technology trends, Device and interconnect scaling, Interconnect Models: RC model and RLC model, Effect of capacitive coupling, Effect of inductive coupling, Transmission line model, Power dissipation, Interconnect reliability, Driver and Load Device Models, Interconnect Analysis, Time domain analysis, RLC network analysis, RC network analysis and responses in time domain, S domain analysis, Circuit reduction via matrix approximation, Analysis using moment matching, Crosstalk Analysis, Advanced Interconnect Materials. Moore law, Technology nodes and ITRS, Physical & Technological Challenges to scaling, Two terminal MOS Device threshold voltage modelling, C-V Characteristics, Four terminal MOSFET threshold voltage I-V modelling, Short channel effect (SCE), High-K gate dielectric, Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs). Nonconventional MOSFET – (FDSOI, SOI, Multi-gate MOSFETs) and advanced VLSI devices and interconnects |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-052 |
| 3 | **Title of the subject** | VLSI Signal Processing |
| 4 | **Any prerequisite** | Digital Circuit, and Signals & Systems |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | This course aims at providing comprehensive coverage of the important techniques for designing efficient VLSI architectures for DSP. This course will enable students to understand industrial challenges in the implementation of DSP systems, like capability to process high throughput data in real-time, as well as requiring less power and less chip area. |
| 7 | **Brief Contents** | Graphical representation of DSP algorithms, Signal flow graph (SFG), Data flow graph (DFG) and dependence graph (DG), High-level transformation, Critical path, Retiming of DFG, Critical path minimization by retiming, Loop retiming and iteration bound, Cutset retiming, Design of pipelined DSP architectures. Parallel realization of DSP algorithms, Unfolding theorem, Polyphase decomposition, Hardware efficient parallel realization of FIR filters, 2-parallel and<br>3-parallel filter architectures, Hardware minimization by folding, Delay optimization by folding, Lifetime analysis. Pipelining digital filters, Combining parallel processing with pipelining in digital filters and for advanced VLSI signal processing. |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-053 |
| 3 | **Title of the subject** | Low Power VLSI |
| 4 | **Any prerequisite** | Digital Electronics |

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|---|---|---|
| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | Correctly describe the detailed behaviour of given digital logic circuits as defined by Verilog HDL, state diagrams, or other means, including those circuits related to modern computer architecture.<br>Translate system requirements into a practical digital design, making use of modern engineering tools such as Xilinx Vivado, Verilog HDL, and FPGA prototyping boards.<br>Demonstrate the ability to modify existing HDL code to meet new system requirements.<br>Demonstrate hands-on test bench and prototyping skills to ensure that a design meets the specified system requirements. |
| 7 | **Brief Contents** | Introduction: Need for low-power VLSI chips, Sources of power dissipation on Digital Integrated circuits, Dynamic dissipation, Static Dissipation, Technology & Device innovation, Emerging Low power approaches, Low power design techniques at architecture and system levels, Power consumption of dedicated hardware vs. software implementations of systems, Low power architecture, RTL design techniques for low power, UPF, Low power random access memory circuits, Power analysis and design at system level and state-of-the-art low power applications |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-054 |
| 3 | **Title of the subject** | Microcontroller and Embedded System |
| 4 | **Any prerequisite** | Nil |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | This course aims to convey knowledge of basic concepts of embedded system design required for every state-of-the-art electrical/electronic system in the form of autonomous and real–time computing machine embodied within them. Emphasis is on the features and characteristics of embedded system, design metrics, embedded system design flow, processor, memory and input output interfacing and input output devices, assembly language, hardware description language, I/O interface design and programming, real-time operating system, hardware-software co-design and co-simulation. Special attention will be devoted to the most important challenges facing embedded system designers today and in the coming decade. |
| 7 | **Brief Contents** | Introduction to Real Time Embedded System; Embedded system, Real time, Conventional architecture, Major components of ESD, Design issues, Design metrics and Design methodology, Task level design approach, structural layout, Structure of ES, ASIC Microprocessor, DSP, Microcontroller, ASIC, Memory and FPGA Introduction to Computing, 8051 Microcontroller developed by Intel, 8051 interfacing to external memory, LCD, ADC and sensors, Advanced microcontroller: ARM University program: ARM architecture fundamentals., State-of-the-art Processor, FPGA (Virtex-7 series, ZedBoard, Basys 3 Artix-7), DSP, Microcontroller, ASIC and Memory chips used in various real time embedded autonomous and intelligent applications. |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-055 |
| 3 | **Titleofthesubject** | MemoryDevices and Circuits |
| 4 | **Anyprerequisite** | Digital Electronics |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectivesof the subject** | The objective of the Memory Design is to acquaint the students with memory cells,memory peripherals, novel SRAM cells, next-generation memory, memory architecture, memory structure in processing unit. Thesubject gives the platform to analyze the read/write/hold operations of different memorystructuresusingCAD tools. |
| 7 | **Brief Contents** | Overview of volatile memory, Non-volatile memory, On-chip memory, On-chip memorytypes.ReviewofCMOScircuitdesign,Sensingcircuitrybasics,Read/ writeassistcircuitryand otherperipheralcircuitries,NextgenerationSRAM cell. IntroductiontoDRAM,HighspeedDRAMarchitectures,Openandfoldedarray sorganizations,Bandwidth,latency,and Cycletime, Power,Timingcircuits. STT-MRAM,Data migrationpolicyforhybridcache. OperationofFLASHmemories(FLASHarraysensingandprogramming),Char gePump circuits. Basic of memory compiler for SRAM architecture using scripting language, Memory unit in MPU/MCU. |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-056 |

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| 3 | **Titleofthesubject** | VLSIArchitecture |
| 4 | **Anyprerequisite** | System Design using HDL |
| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectivesof the subject** | Thecourseobjectiveistocoverthearchitecturedesignof VLSIsystems andsubsystems with the notion of optimization for area, speed, powerdissipation, costandreliability.DifferentaspectsofVLSIsystemdesign anditsapplicationsinvariousfield.Thecoursealsodiscussestraditionaland stateoftheartanalogand digitalVLSIarchitecturesoptimizedtechniques. |
| 7 | **BriefContents** | ISA, Datapath and control path design, Single Cycle MIPS , 5 Stage pipeline MIPS, CISC Architecture, RISC architecture, Arithmetic unit design, Fixed point and floating point, memory units, Optimization, Instruction level parallelism, Super scalar processor, Multi-core and multi thread Architecture, Network on chip, Dynamicallyreconfigurablegatearray, Staticvsdynamicreconfiguration, Single context vs multi-context dynamic reconfiguration, Full vspartialrun time reconfiguration. |

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|---|---|---|
| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-057 |
| 3 | **Titleofthesubject** | HardwareSecurity |
| 4 | **Anyprerequisite** | VLSIDesign |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **LearningObjectives of the subject** | Learningthestate-of-the-artsecuritymethodsanddevices, betterunderstandingofattacksandprovidingcountermeasuresagainstthem, CMOS implementation of hardware security primitives, Attacks on cyber-physical systems |
| 7 | **Brief Contents** | ModuleI:FundamentalsofhardwaresecurityandtrustforintegratedcircuitsPhysical and invasive attacks, Side-channel attacks and Countermeasures, Physicallyunclonablefunctions,Hardware-based true randomnumber generators, Hardware Trojan, Hardware security primitives, CMOS PUF implementations<br><br>ModuleII:WatermarkingofIntellectualProperty(IP)blocks,FPGAsecurity, Passive and active metering for prevention of piracy, Access control, Hardware Trojandetectionand isolationinIPcoresandintegrated circuitscounterfeitICs |

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| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-058 |
| 3 | **Title of the subject** | FPGA Based System Design |
| 4 | **Any prerequisite** | Nil |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectives of the subject** | The goal of the course is to study the basic principles and methods of FPGA prototyping.<br>Understanding of principles of IC prototyping; hardware and software; design strategies and methods |
| 7 | **Brief Contents** | ROM, SPLD, CPLD Architecture and Features of FPGA and designing techniques.<br>Architecture of ROM – ROM Programming – Architecture of SPLDs – SPLDs programming – Architecture of CPLDs – Basics of FPGAs– Structure of FPGAsImplementation of Digital circuits in FPGA processor, Education FPGA kit – FPGA pin assignment – Interfacing Input/Output devices with FPGA, SPI, I2C, I3C, UART protocol RTL designSystem Design Examples using Xillinx FPGAs – Traffic light Controller, Real Time Clock, VGA, Keyboard, LCD, Embedded Processor Hardware Design |

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| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-059 |
| 3 | **Title of the subject** | Quantum electronics |
| 4 | **Any prerequisite** | Digital IC Design |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | The course gives an introduction to solid state physics, and will enable the student to employ classical and quantum mechanical theories needed to understand the physical properties of solids. Emphasis is put on building models able to explain several different phenomena in the solid state. |
| 7 | **Brief Contents** | The crystal structure of solids, Introduction to quantum mechanics: Principles of Quantum mechanics, Application of Schrodinger's Wave Equations, Introduction to Quantum Theory of Solids: The kronig-Penney Model, Electrical conduction in Solids, DOS, Statistical Mechanics, The semiconductor in Equilibrium Carrier transport Phenomenon, Non-equilibrium Excess Carriers in Semiconductor, PN-Junction, MOSCAP, Thin film Transistors, QCA |

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| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-060 |
| 3 | **Title of the subject** | RF Circuit Design |
| 4 | **Any prerequisite** | Analog IC Design |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectives of the subject** | Get the idea of various parameters of interest in RF systems. To understand issues involved in design for GHz frequencies. To understand theoretical background relevant for design of active and passive circuits for RF front end in wireless digital communication systems. |
| 7 | **Brief Contents** | Characteristics of passive components for RF circuits. Passive RLC networks. Transmission lines. Two-port network modeling. S-parameter model. The Smith Chart and its applications, Active devices for RF circuits: SiGe MOSFET, GaAs pHEMT, HBT and MESFET. RF Amplifier design: single and multi-stage amplifiers. Review of analog filter design. Voltage references and biasing. Low Noise Amplifier design: noise types and their characterization, LNA topologies, Power match vs Noise match. Linearity and large-signal performance, RF Power amplifiers: General properties. Class A, AB and C Power amplifiers. Class D, E and F amplifiers. Modulation of power amplifiers, Analog communication circuits, Phase-locked loops, Oscillators and synthesizers. |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-061 |
| 3 | **Titleofthesubject** | Mixed Signal SoC Design |
| 4 | **Anyprerequisite** | Analog IC Design |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectivesof the subject** | Attheend ofthecoursethestudent willbeableto:<br>Understandthesignificanceofdifferentbiasingstylesandapplythemaptlyfordifferentcircuits.<br>Designbasicbuildingblockslikesources,sinks, mirrors,uptolayoutlevel.<br>ComprehendthestabilityissuesofthesystemsanddesignOp-ampfullycompensated againstprocess,supplyand temperaturevariations.<br>Identifysuitabletopologiesoftheconstituentsubsystemsandcorrespondingcircuitsasperthe specificationsofthe system<br>DesignAnalogintegratedsystemincludingparasiticeffectsuptotape-out. |
| 7 | **BriefContents** | Process and temperature independent compensation, Resistor Equivalence of a Switched Capacitor, Parasitic-Sensitive Integrator, Parasitic-Insensitive Integrators, Signal-Flow-Graph Analysis, Noise in Switched-Capacitor Circuit.<br>Performance of Sample-and-Hold Circuits, Ideal D/A Converter, Ideal A/D Converter, Quantization Noise, Charge-Redistribution A/D, Resistor-Capacitor Hybrid, Basic Phase-Locked Loop Architecture, Voltage Controlled Oscillator, Divider Phase Detector, Loop Filer, PLL in Lock, Linearized Small-Signal Analysis, Second-Order PLL Model , Jitter and Phase Noise, Period Jitter, Probability Density Function of Jitter, Ring Oscillators, LC Oscillators, phase Noise of Oscillators, jitter and Phase Noise in PLLS, |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-062 |
| 3 | **Titleofthesubject** | AI-Accelerator Design |
| 4 | **Anyprerequisite** | NIL |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectivesof the subject** | This course provides in-depth coverage of the architectural techniques used to design accelerators for training and inference in machine learning systems.<br>Get exposure of implementation of CNN network in FPGA board.<br>Get an idea about data system bus used in communication between different system blocks.<br>To design energy-efficient accelerators, develop the intuition to make trade-offs between ML model parameters and hardware implementation techniques. |
| 7 | **BriefContents** | Deep understanding of Neural networks, Linear algebra fundamentals and accelerating linear algebra, Implementation of Deep Learning Kernels, Zynq series FPGA architecture, interface knowledge, high speed protocol (Ethernet 100/10 Gbps), c/c++ coding for Vivado SDK, activation function verilog implementation, classification layer HDL implementation, SPI, I2C, I3C, UART protocol RTL design. |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-063 |
| 3 | **Titleofthesubject** | System-on-Performance Chip Design |
| 4 | **Anyprerequisite** | NIL |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectivesof the subject** | This course provides in-depth coverage of System-on-Performance Chip Design. Design, optimize, and program a modern System-on-a-Chip to analyse and characterize its computational requirements computational task, and identify performance bottlenecks. Characterize and develop real-time solutions. Implement both hardware and software solutions, formulate hardware/software tradeoffs, and perform hardware/software codesign. |
| 7 | **BriefContents** | Architectural building blocks and heterogeneous architecture, Hardware-Software Codesign, Embedded Software, Interfacing, Computational requirements and system analysis, Concurrency, Real Time, Design-space formulation and exploration, Costs and metrics (energy, area, runtime, reliability, predictability), Quantitative design and analysis. |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-064 |
| 3 | **Titleofthesubject** | Embedded Software |
| 4 | **Anyprerequisite** | Nil |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectivesof the subject** | Analyze and explain the control-flow and data-flow of a software program and acycle-based hardware description.<br>Transformsimplesoftwareprogramsintocycle-basedhardwaredescriptionswithequivalentbehaviorandvice versa.<br>Partitionsimplesoftwareprogramsintohardwareandsoftwarecomponents,andcreateappropriatehardware-softwareinterfacesto reflectthispartitioning.<br>Identifyperformancebottlenecksinagivenhardware-softwarearchitectureandoptimizethembytransformationsonhardwareand softwarecomponents. |
| 7 | **Brief Contents** | Design of embedded systems, Architectures and platforms for embedded systems, General purpose vs.applicationspecificarchitectures,ReconfigurableSystems, Modeling techniques, Models of computations, Synchronous finite statemachines, Time and synchrony, Co-designfinitestatemachines,Systemdesign withthePOLISsystem, Performanceanalysisandco-simulation, Staticanalysistechniques,Co-simulationofheterogeneoussystemswithPtolemy, Optimizationtechniquesfordesignspaceexploration, Software synthesis and code generation, Retargetable compilers, System-level power/energy optimization Mappingandschedulingforlowenergy, Real-timescheduling withdynamicvoltagescaling. |

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| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-065 |
| 3 | **Title of the subject** | High Performance Computing Systems |
| 4 | **Any prerequisite** | VLSI Architecture |
| 5 | **L-T-P** | 3-0-0 |

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| 6 | **Learning Objectives of the subject** | To get in-depth analysis of issues in High Performance Computing systems including: (1) Parallel Computing (2) New Processor Architectures, (3) Power-Aware Computing and Communication, (4) Advanced Topics on Peta scale Computing and Optical Systems.<br>To understand parallel models of computation such as dataflow, and demand-driven computation. |
| 7 | **Brief Contents** | Parallel Processing Concepts; Levels and model of parallelism: Instruction, Transaction, Task, Thread, Memory, Function, Data Flow models, Demand-driven computation; Parallel architectures: Superscalar architectures, Multi-core, Multi-threaded, Server and cloud; Fundamental design issues in HPC: Load balancing, scheduling, Synchronization and resource management; Operating systems for scalable HPC; Parallel languages and programming environments; Fundamental limitations in HPC, Benchmarking HPC, Scalable storage systems, Accelerated HPC, Power-aware HPC Design. |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-066 |
| 3 | **Titleofthesubject** | Special Topics in IC Design and Technology |
| 4 | **Anyprerequisite** | NIL |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectivesof the subject** | This will focus on special topics of contemporary relevance and interest to both VLSI industry and state-of-the-art research. |
| 7 | **BriefContents** | It will cover current research and development topics and in line with VLSI industry and may cover all aspects from Device Technology to chip design flow through ASIC and FPGA. |

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| 1 | **Type of course** | Elective |
| 2 | **Code of the subject** | EE-067 |
| 3 | **Title of the subject** | Sensors for Autonomous System |
| 4 | **Any prerequisite** | Nil |

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| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | Acquire knowledge about Micro Sensors, Get the idea about sensor application for autonomous system, sensor technology for real-time applications.<br>Modern control methods that can be used to mathematically model or estimate the function of real systems, A range of autonomous decision-making approaches, including optimization to ensure desired outcomes |
| 7 | **Brief Contents** | Introduction and historical background, Microsensors : Sensors and characteristics, Integrated Smart sensors, Sensor Principles/classification-Physical sensors.<br>Methods for data acquisition, and issues associated with different techniques (e.g. Nyquist, noise, etc.), modelling dynamic systems using transfer functions, with a particular focus on electro-mechanical systems, multiple-input-multiple-output systems, feedback control methods using observability and parameter estimation, rule based and optimization approaches, hardware development, system dependability (reliability, availability and safety); fault detection, diagnosis and prognosis |

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| 1 | **Type of course** | Elective |
| 2 | **Codeofthesubject** | EE-068 |
| 3 | **Titleofthesubject** | Network on Chip |

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| 4 | **Anyprerequisite** | NIL |
| 5 | **L-T-P** | 3-0-0 |
| 6 | **Learning Objectives of the subject** | Upon completion of this course, students will be able to:incorporatehundreds of cores into a single chip, Router microarchitecture, Flow control, Routing algorithms, Designing Power efficient NoC, Three dimensional networks-on-chiparchitectures, Analyze test and fault tolerance of Communications in NOC, Apply the 3D Integration procedures in NOC |
| 7 | **Brief Contents** | Introduction to NoC, OSI layer rules in NoC, Interconnection Networks in Network-on-Chip Network Topologies, Switching Techniques, Routing Strategies, Architecture Design, Switching Techniques and Packet Format, Asynchronous FIFO Design, Wormhole Router Architecture Design - VC Router Architecture Design - Adaptive Router Architecture Design, Routing Algorithms, Test and Fault Tolerance of NOC, 3-D integration of NOC. |